GIMIX inc. 1337 W. 37th Place Chicago, Ill. 60609 (312) 927-5510

CPU BOARD

The GIMIX GHOST CPU Board is the heart of the GIMIX GHOST computer system. It contains a 6800 microprocessor unit and all the circuits needed for system control. It contains a scratchpad RAM, and logic and sockets for four PROMs. It contains a bit rate generator, a timer, and a clock generator to clock the system and facilitate direct memory access. The CPU Board is fully compatible with the SS50 bus, and may be used as a plug-in replacement in several other systems. Tri-state buffered bus lines allow the Board to be used in multi-processing systems.

FEATURES

-- 6800 MPU, 1MHz standard (1.5 or 2 MHz optional)
-- 6875 clock generator with its own crystal
-- 14411 bit rate generator with its own crystal (110-9600 baud)
-- 6840 timer, switch-addressable to any 8-word boundary
-- 6810 RAM, switch-addressable to any 128-word boundary
-- Sockets for four 2708 PROMs (not included)
-- PROM block switch-addressable to any 4K boundary
-- Dual-address switch lets one PROM respond to both E000 and FC00
-- Split-address strapping places PROMs at E000, E400, E800, FC00
-- PROMs, RAM, and timer tied internally to MPU lines, rather than through the system bus
-- Buffered (and high-impedance when MPU halted): address and data lines, Ø1, BA, R/$\overline{W}$, $\overline{VMA}$
-- Buffered in: $\overline{\text{Manual Restart}}$ (with debounce circuit) and $\overline{\text{Halt}}$
-- Buffered out: Ø2, Reset; 110, 150, 300, 600, 1200 baud (may be restrapped to any of 2400, 4800, 9600)
-- Direct in (with 6.8K pullups): $\overline{IRQ}$, $\overline{NMI}$
-- DMA capability through cycle stealing, or halting the MPU
-- Four voltage regulators
-- .8A current requirement (1.5A max), without 2708s
-- Plugs into SS50 mother board

CONNECTIONS

The Board is factory-strapped for five standard bit rates. See Fig. 1 for an example of 2400 baud being available in place of 110.

The RAM is controlled by switch bank S2. Turn ON switch 10 to enable the RAM. Set switch 1-9 to match bits A7-15 (in that order) of the address desired. See Fig. 2 for an example.

The timer is controlled by banks S3-4. Turn ON switch 6 of S4 to enable; turn ON switch 7 (or 8) to tie the interrupt request to the MPU's $\overline{NMI}$ (or $\overline{IRQ}$). Set the other switches to match bits A3-15 of the address desired. See Fig. 3 for an example. Also see logic diagram for timer functions available at the J1 connector.

The PROM block is controlled by bank S1, as illustrated in Fig. 4. PROM selection depends on the values on lines A11-10, in that a LOW is placed on pin 20 of socket U7 or U8 or U9, or on pad EC or FC. In the latter case, a jumper is needed to select U6 or U9. Selection takes place as follows:

If switch 1 is OFF--

(a) and lines A12-15 do not match switch 2-5: no selection.

(b) and lines A12-15 match switch 2-5: socket or pad selected as in Table 1.

If switch 1 is ON--

(c) and switch 2 is OFF: no selection (use this combination to disable PROMs).

(d) and switch 2 is ON, but lines A13-15 do not match switch 3-5: no selection.

(e) and switch 2 is ON, and lines A13-15 match switch 3-5: socket or pad selected as in Table 2.

Note the memory map of upper 8K in Table 3. It shows that any addressable devices (ROMs, RAMs, PIAs, etc) may be placed in the range F000-FBFF in case of dual address (Fig. 4C) or split address (Fig. 4D). In the latter case, the on-board RAM or timer (but nothing else) may be placed at EC00-EFFF.

Direct memory access may be accomplished by strapping, one possibility being shown in Fig. 5. Use jumpers to tie bus UD1 and UD2 to RG, DR, MR as desired. If CS is tied to RG (instead of to ground), the bus lines will be in high-impedance state as soon as MR goes high. (Use of pullup resistors, as provided on the GIMIX mother board, will force BA high.) See the 6875 specifications for timings.

Multiprocessing may be accomplished by holding low the $\overline{\text{Halt}}$ line. As soon as BA goes high, the MPU is halted and the bus is in high impedance state; then the other MPU may take control of the bus.

Table 1

A11	A10	select
0	0	U9
0	1	U8
1	0	U7
1	1	EC

Table 2

A12	A11	A10	select
0	0	0	U9
0	0	1	U8
0	1	0	U7
0	1	1	EC
1	0	0	none
1	0	1	"
1	1	0	"
1	1	1	FC

Table 3

	dual	split
FC00	U9	U6
F800	*	*
F400	*	*
F000	*	*
EC00	U6	**
E800	U7	U7
E400	U8	U8
E000	U9	U9

* any devices

** no devices except CPU Board's own 6810, 6840

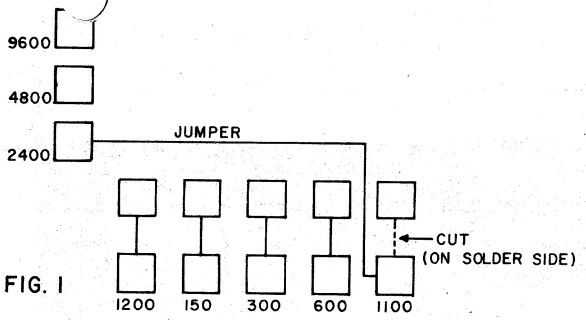


FIG. 1

RAM ENABLED AT A000

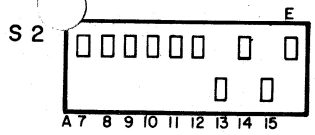


FIG. 2A

RAM DISABLED

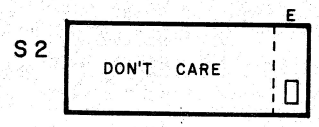


FIG. 2B

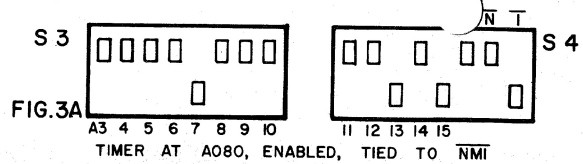


FIG. 3A

TIMER AT A080, ENABLED, TIED TO $\overline{NMI}$

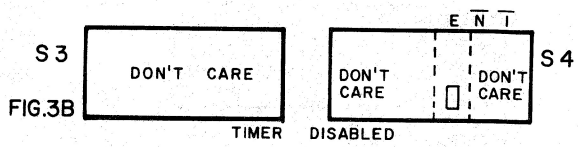


FIG. 3B

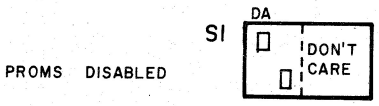


FIG. 4A

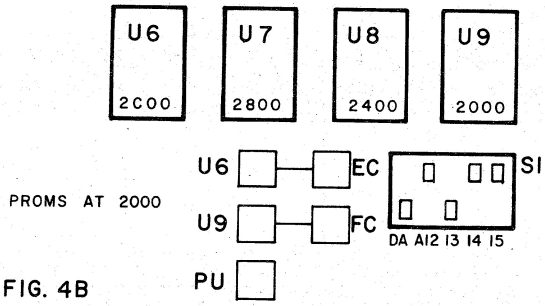


FIG. 4B

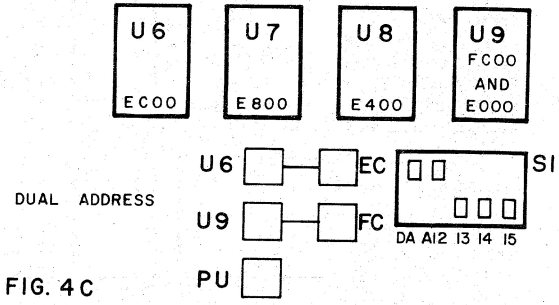


FIG. 4C

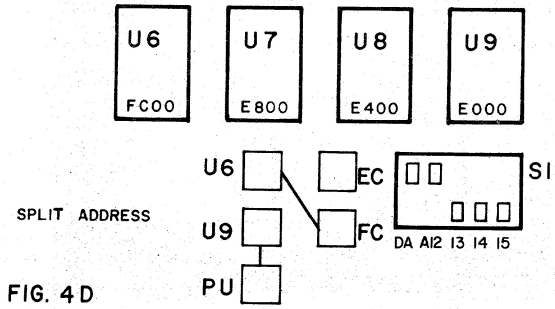


FIG. 4D

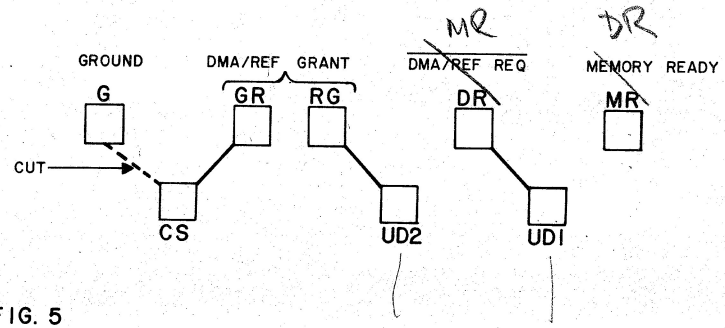
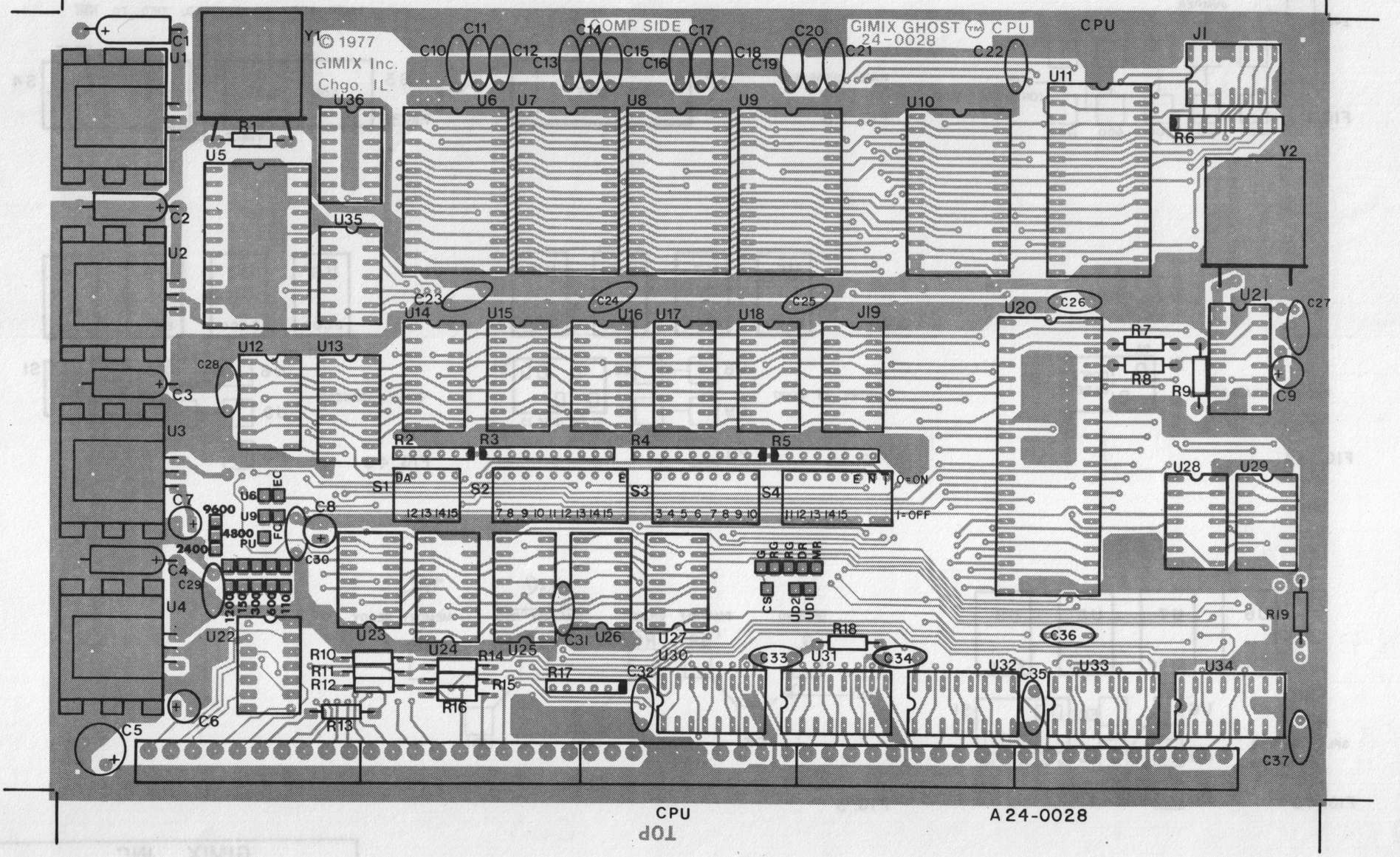
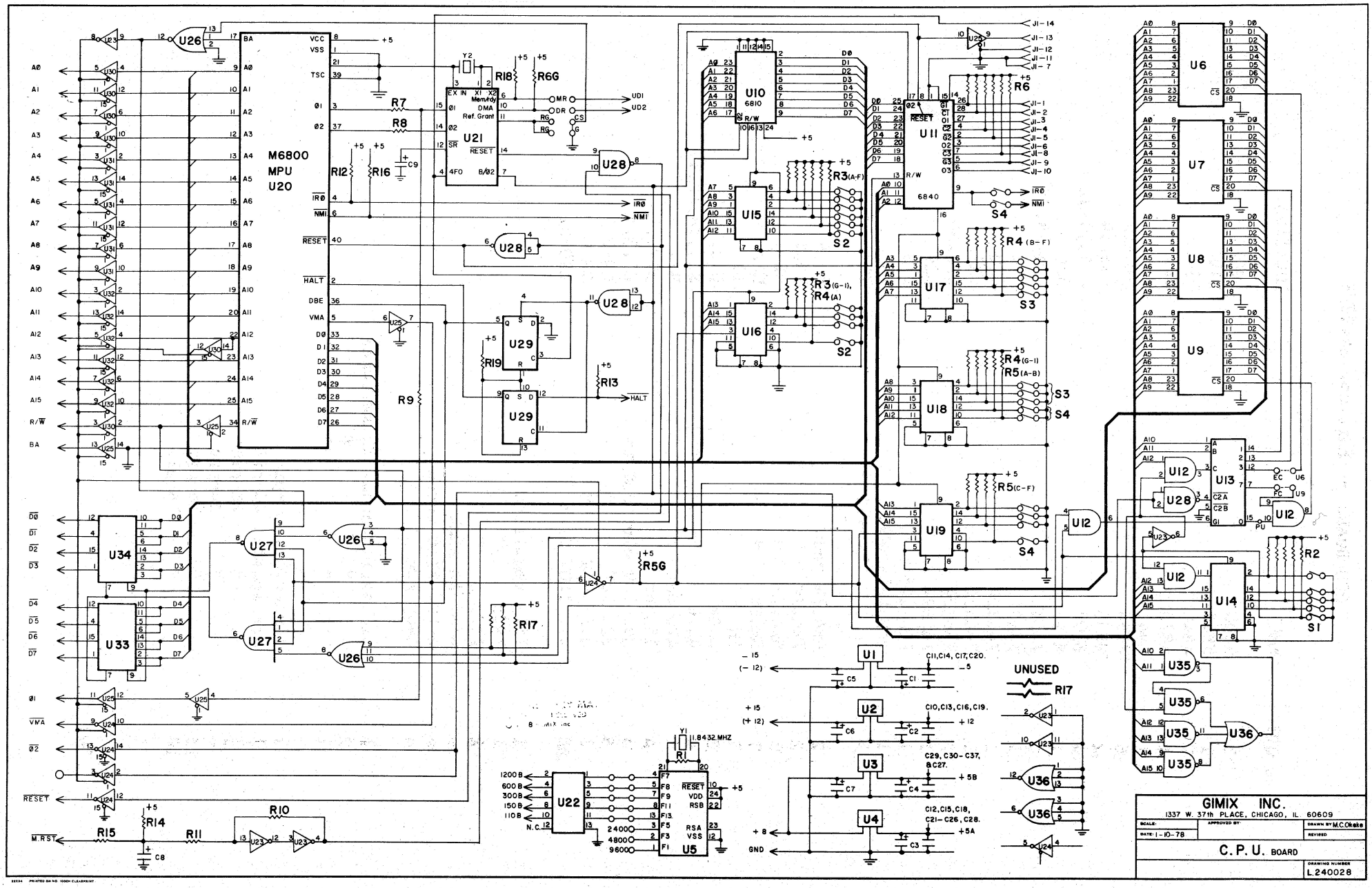


FIG. 5

GIMIX INC. 1337 W. 37th PLACE, CHICAGO, IL. 60609.		
SCALE:	APPROVED BY:	DRAWN BY M.C.Okeke
DATE: 1-13-78		REVISED
C.P.U. BOARD SWITCHES AND STRAPPING		
		DRAWING NUMBER D240028


COMP SIDE
GIMIX GHOST ™ CPU
24-0028
CPU
© 1977
GIMIX Inc.
Chgo. IL
Y1
C1
U1
R1
U36
U6
U7
U8
U9
U10
U11
J1
R6
Y2
U5
C2
U2
U35
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
U14
U15
U16
U17
U18
J19
U20
C26
U21
C27
R7
R8
R9
C9
U12
U13
C28
C3
U3
R2
R3
R4
R5
S1
S2
S3
S4
ON
OFF
U28
U29
C7
C8
C30
C4
C29
U4
U22
U23
U24
U25
C31
U26
U27
U30
R10
R11
R12
R13
R14
R15
R16
R17
R18
C32
C33
U31
C34
U32
C35
U33
U34
C36
R19
C37
C5
C6
CPU
A24-0028
TOP


M6800
MPU
U20
U21
U10
6810
U11
6840
U15
U16
U17
U18
U19
U6
U7
U8
U9
U12
U13
U14
U26
U27
U28
U29
U34
U33
U22
U5
U1
U2
U3
U4
U35
U36
S1
S2
S3
S4
R1
R2
R3 (A-F)
R3 (G-I), R4 (A)
R4 (B-F)
R4 (G-I) R5 (A-B)
R5 (C-F)
R5G
R6
R6G
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
Y1 8.832 MHZ
C11, C14, C17, C20. -5
C10, C13, C16, C19. +12
C29, C30 - C37, &C27. +5B
C12, C15, C18, C21 - C26, C28. +5A
UNUSED
R17
GIMIX INC.
1337 W. 37th PLACE, CHICAGO, IL 60609
C.P.U. BOARD
DRAWN BY M.C.Okeke
DATE: 1-10-78
L.240028

CPU BOARD -- Part no. 24-0028

QTY	PART	LOCATION
1	6800	U20
1	6810A	U10
1	6840	U11
1	6875	U21
1	14411	U5
6	8136	U14-19
2	8835	U33,34
4	8T97	U25,30-32
1	8T98	U24
3	74LS00	U12,28,35
1	74L04	U22
1	74LS04	U23
1	74LS20	U27
2	74LS27	U26,36
1	74LS74	U29
1	74LS138	U13
1	crystal, 4MHz	Y2
1	" 1.8432	Y1
2	9x4.7k pack	R3,4
2	7x4.7k "	R5,6
1	5x4.7k "	R2
1	5x680 "	R17
1	1M	R1
3	6.8k	R10,12,16
4	4.7k	R13,14,18,19
1	470 ohm	R11
4	15 ohm	R7-9,15
3	39, 10V electrolyte	C1,3,4
5	22, 16V "	C5-9
1	4.7, 15V "	C2
28	.1, 100V disc	C10-37
1	7812 regulator	
1	7905 "	
2	7805 "	
4	6107-14 sink	
4	4-40, 5/16 screw	
4	4-40 nut	
1	DIP switch bank, 10 switches	
2	" 8	
1	" 5	
1	connector, 50-pin	
1	DIP socket, 40-pin	
1	" 28-pin	
6	" 24-pin	
15	" 16-pin	
10	" 14-pin	